HP 8xSFF backplane 496074-001 - block diagram of what is known

Two PIC18F24K20 per board (PIC A = bays 1-4, PIC B = bays 5-8). The PICs only handle LEDs, drive-detect and the sideband: SAS data never touches them.

POWER / SIDEBAND CONNECTOR J13

Mini-Fit Jr 2x5 (details: sheet 7)

pin 9	address strap *PIC A direct, PIC B via 750 ohm*
pin 6, 10	+5 V *-> 3V3 regulator*
pin 3 / 8	I2C SCL / SDA *both PICs*
pin 1, 5	+12 V *-> drive power*
pin 2, 4, 7	GND

pin 9 -> PIC A RA0 direct; PIC B RA0 via 750 ohm

5 V -> 3V3

TC1264 LDO

3.3 V 800 mA

SOT-223

+3V3 -> VDD (pin 20) of both PICs

SCL+SDA

J44 (0.1" header)

1 SDA 2 GND 3 SCL

same bus as the power connector

ESP32: SDA=GPIO21 SCL=GPIO22

J14 (U1) / J43 (U2, unpopulated)

pin 1 GND, pin 2 -> 10 k -> PIC pin 26 (RB5)

purpose unknown: test / debug tap?

J43 pin 1 not traced

ICSP headers J11 / J12

J11 -> PIC A, J12 -> PIC B (confirmed)

MCLR, VDD, VSS, PGD=RB7, PGC=RB6

ICD4 holds PIC in reset; does not power it

I2C bus

(pulled up on board)

custom fw: 0x30/31 or 0x32/33

PIC18F24K20

PIC A

bays 1-4

RC3/RC4 I2C slave

RA0 strap, direct from pin 9

RA1 AN1 (source not found)

RB0-2 / RC5 SGPIO

4 x drive-detect in

12 x LED out (active low)

SGPIO

J1 (IPASS1) SFF-8087

4 SAS lanes -> bays 1-4

feeds PIC A + bays 1-4

(assignment from Ben, silkscreen)

```
sideband (backplane end):
A8 SClock -> RB2
A9 SLoad -> RB0
B10 SDataOut -> RB1
B11 SDataIn <- RC5
```

SAS

PIC18F24K20

PIC B

bays 5-8

RC3/RC4 I2C slave

RA0 strap via 750 ohm

RA1 AN1 (source not found)

RB0-2 / RC5 SGPIO

4 x drive-detect in

12 x LED out (active low)

SGPIO

J6 (IPASS2) SFF-8087

4 SAS lanes -> bays 5-8

feeds PIC B + bays 5-8

(assignment from Ben, silkscreen)

```
sideband (backplane end):
A8 SClock -> RB2
A9 SLoad -> RB0
B10 SDataOut -> RB1
B11 SDataIn <- RC5
```

DRIVE BAY 1 *drive-detect + 3 LEDs*

2 x 100 uF on this drive's 5 V / 12 V rails

act loc err

DRIVE BAY 2 *drive-detect + 3 LEDs*

2 x 100 uF on this drive's 5 V / 12 V rails

act loc err

DRIVE BAY 3 *drive-detect + 3 LEDs*

2 x 100 uF on this drive's 5 V / 12 V rails

act loc err

DRIVE BAY 4 *drive-detect + 3 LEDs*

2 x 100 uF on this drive's 5 V / 12 V rails

act loc err

DRIVE BAY 5 *drive-detect + 3 LEDs*

2 x 100 uF on this drive's 5 V / 12 V rails

act loc err

DRIVE BAY 6 *drive-detect + 3 LEDs*

2 x 100 uF on this drive's 5 V / 12 V rails

act loc err

DRIVE BAY 7 *drive-detect + 3 LEDs*

2 x 100 uF on this drive's 5 V / 12 V rails

act loc err

DRIVE BAY 8 *drive-detect + 3 LEDs*

2 x 100 uF on this drive's 5 V / 12 V rails

act loc err

LINE STYLE = HOW WELL IT IS KNOWN

- verified on the real board (buzzed / hot-swapped / seen live)
- inferred (disassembly, standards, matched traces) - not tested
- not traced / unknown

Each bay: 3 LEDs driven by its PIC (active low) and 1 drive-detect line (low = drive present) read by the PIC.
Drive ACTIVITY is not wired to any PIC input. Only the SGPIO sideband (inferred) can drive the activity LED; NAS OS drives it from I/O counters instead.

+12 V / +5 V go straight to the drive connectors (not via the PICs). SAS lanes go from each SFF-8087 to its four drives.

HP 8xSFF SAS backplane 496074-001 (DL380 G7)

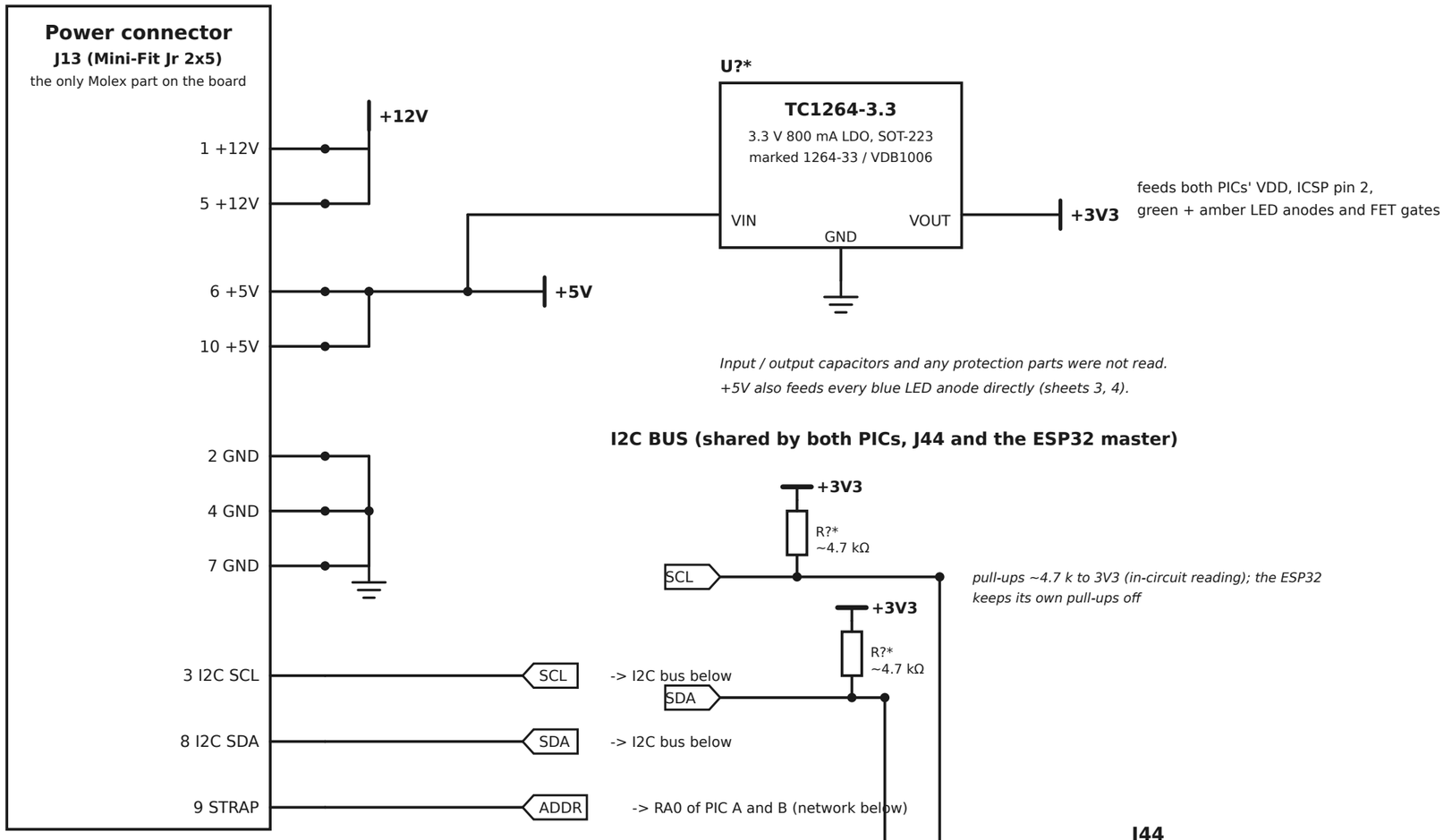
Reverse-engineered functional schematic - NOT the manufacturer's

Sheet 1/9: System overview / block diagram

Drawn 2026-11-05 from bench work 2026-11-04/05

Power, I2C bus, strap and drive power - component level

Shared by both PICs. Net flags (pentagons) continue on sheets 3 and 4.

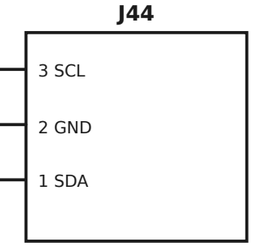


feeds both PICs' VDD, ICSP pin 2,
green + amber LED anodes and FET gates

Input / output capacitors and any protection parts were not read.
+5V also feeds every blue LED anode directly (sheets 3, 4).

I2C BUS (shared by both PICs, J44 and the ESP32 master)

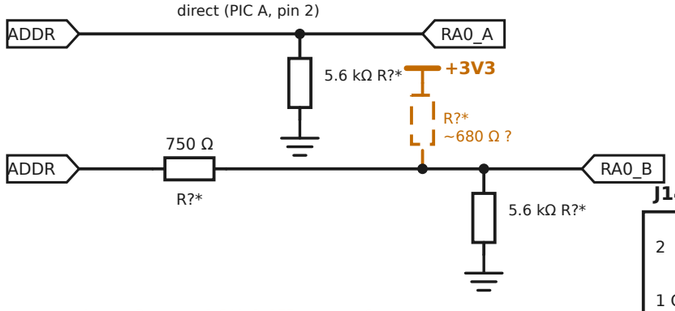
pull-ups ~4.7 k to 3V3 (in-circuit reading); the ESP32 keeps its own pull-ups off



ESP32 (bay controller):
SDA = GPIO21, SCL = GPIO22,
needs a common GND

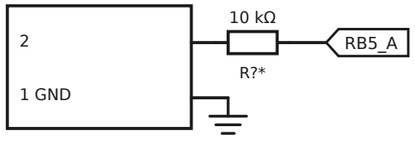
STRAP INPUT NETWORK (connector pin 9 -> RA0 of each PIC)

in-circuit measurements by Ben, 2026-11-05; the pull-up is inferred

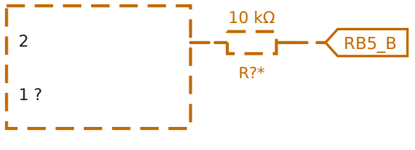


pull-up inferred: B reads ~1.6 V (0x1FE) with pin 9 grounded, which 750 Ω + 5.6 kΩ to ground cannot produce on its own

J14 (pins fitted)



J43 (not fitted)



pin 2 -> 10 k -> pin 26 (RB5) of U1 (J14) / U2 (J43); no divider to ground; nothing plugs in

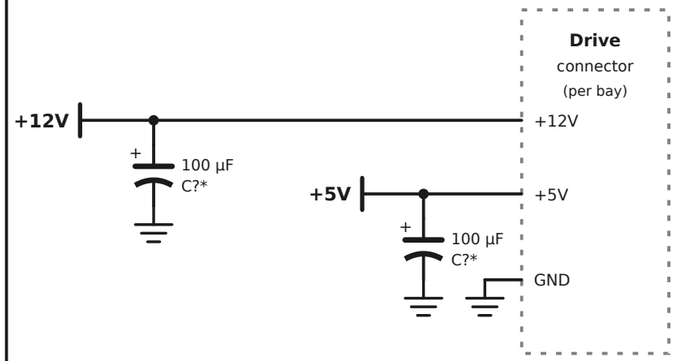
WIRE / OUTLINE STYLE = HOW WELL IT IS KNOWN

- black solid: measured / verified on the real board
- amber dashed: inferred or assumed (e.g. copied from bay 1) - not measured
- grey dotted: not traced / unknown

Designators J1, J6, J11, J12, J13, J14, J43, J44, U1, U2, Q and CR* are from the board (U1 = PIC A, U2 = PIC B).*
*Names ending in * (RB1*, RG2*, RA3* ...) are provisional labels given by this drawing.*

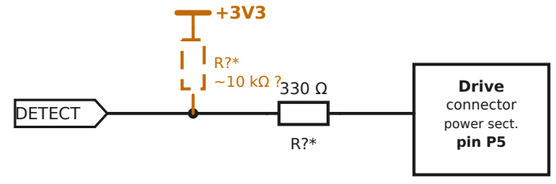
DRIVE POWER (same circuit x8, one per bay)

one 100 µF electrolytic per drive power rail, beside each drive connector



Fuses / hot-plug parts and the SAS lanes were not traced. 12 V and 5 V go straight to the drive connectors, not via the PICs.

DRIVE DETECT (same circuit x8)



P5 is a ground pin on the drive: fitting a drive pulls the node low through 330 Ω. 7.5-10 kΩ measured from P5 to ground in circuit; the pull-up is inferred. DETECT goes to RA7, RA6, RB7, RB6 of each PIC (sheets 3 and 4).

SFF-8087 / ICSP ASSIGNMENT (Ben, 2026-11-05)

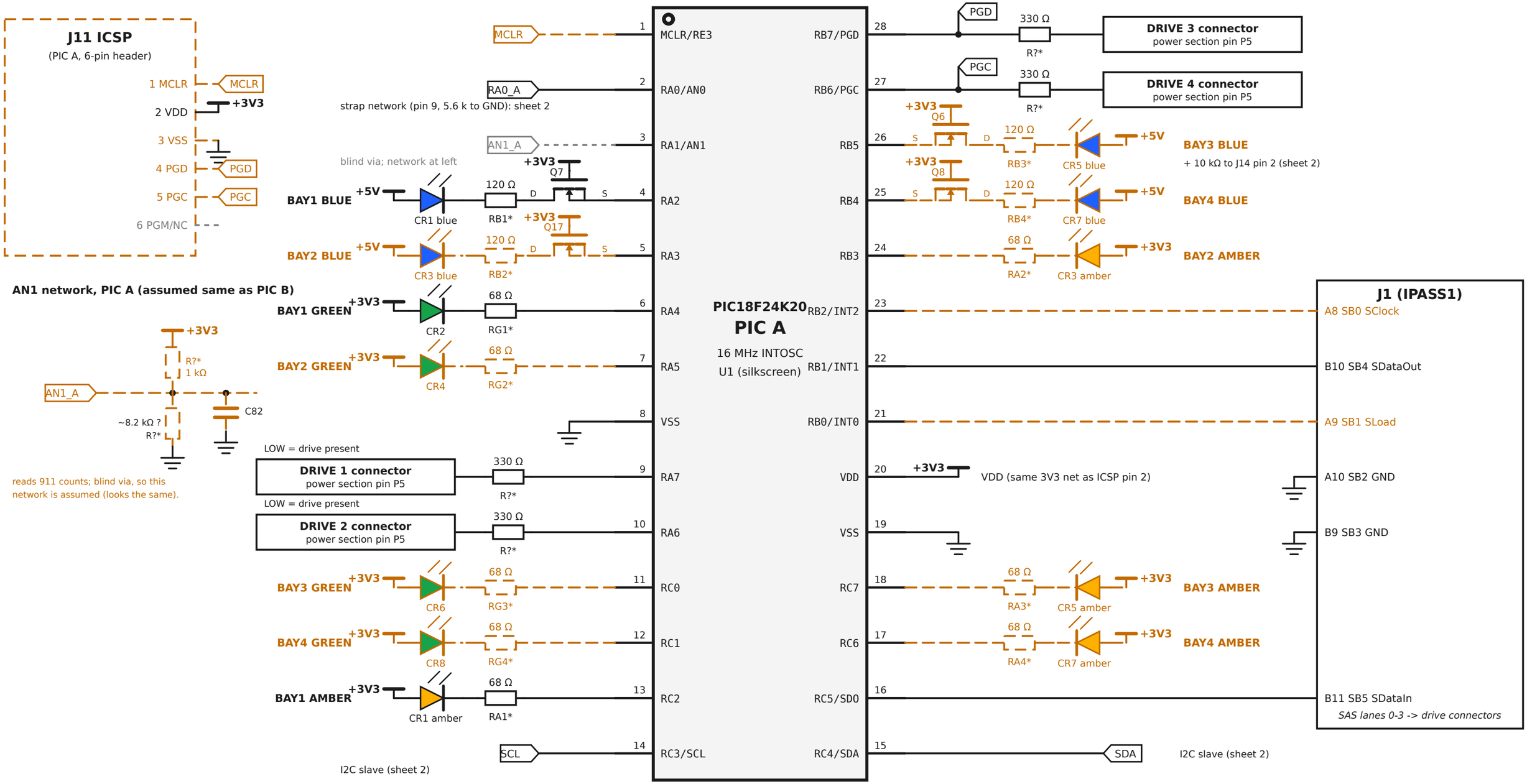
J1 (silkscreen IPASS1) -> PIC A, bays 1-4
J6 (silkscreen IPASS2) -> PIC B, bays 5-8
J11 ICSP -> PIC A
J12 ICSP -> PIC B
Sideband: A8 SClock, A9 SLoad, B10 SDataOut, B11 SDataIn
(sheets 3 and 4 show the PIC end)

HP 8xSFF SAS backplane 496074-001 (DL380 G7)

Reverse-engineered functional schematic - NOT the manufacturer's
Sheet 2/9: Power, I2C and drive power - component level
Drawn 2026-11-05 from bench work 2026-11-04/05

PIC A circuit - PIC18F24K20, J1 (IPASS1) sideband, J11 ICSP, bays 1-4

Bays 1-4. Custom fw I2C 0x30 (backplane 1) / 0x32 (backplane 2). Stock fw 0x76 with power-connector pin 9 grounded.



BLUE: +5V -> LED -> 120 Ω -> FET drain. FET source = PIC pin, gate = +3V3 (fixed). GREEN / AMBER: +3V3 -> LED -> 68 Ω -> PIC pin. All LED pins are active low.

Solid = measured on bay 1 of PIC A only; every other bay is drawn dashed because its values are assumed identical. PGC/PGD share RB6/RB7 with drive-detect lines of bays 3 and 4.

CR1, CR3, CR5, CR7 / CR9, CR11, CR13, CR15 are the dual LEDs (blue and amber dies); CR2, CR4, CR6, CR8 / CR10, CR12, CR14, CR16 are the green LEDs.

WIRE / OUTLINE STYLE = HOW WELL IT IS KNOWN

- black solid: measured / verified on the real board
- amber dashed: inferred or assumed (e.g. copied from bay 1) - not measured
- grey dotted: not traced / unknown

Designators J1, J6, J11, J12, J13, J14, J43, J44, U1, U2, Q and CR* are from the board (U1 = PIC A, U2 = PIC B).*
*Names ending in * (RB1*, RG2*, RA3* ...) are provisional labels given by this drawing.*

HP 8xSFF SAS backplane 496074-001 (DL380 G7)

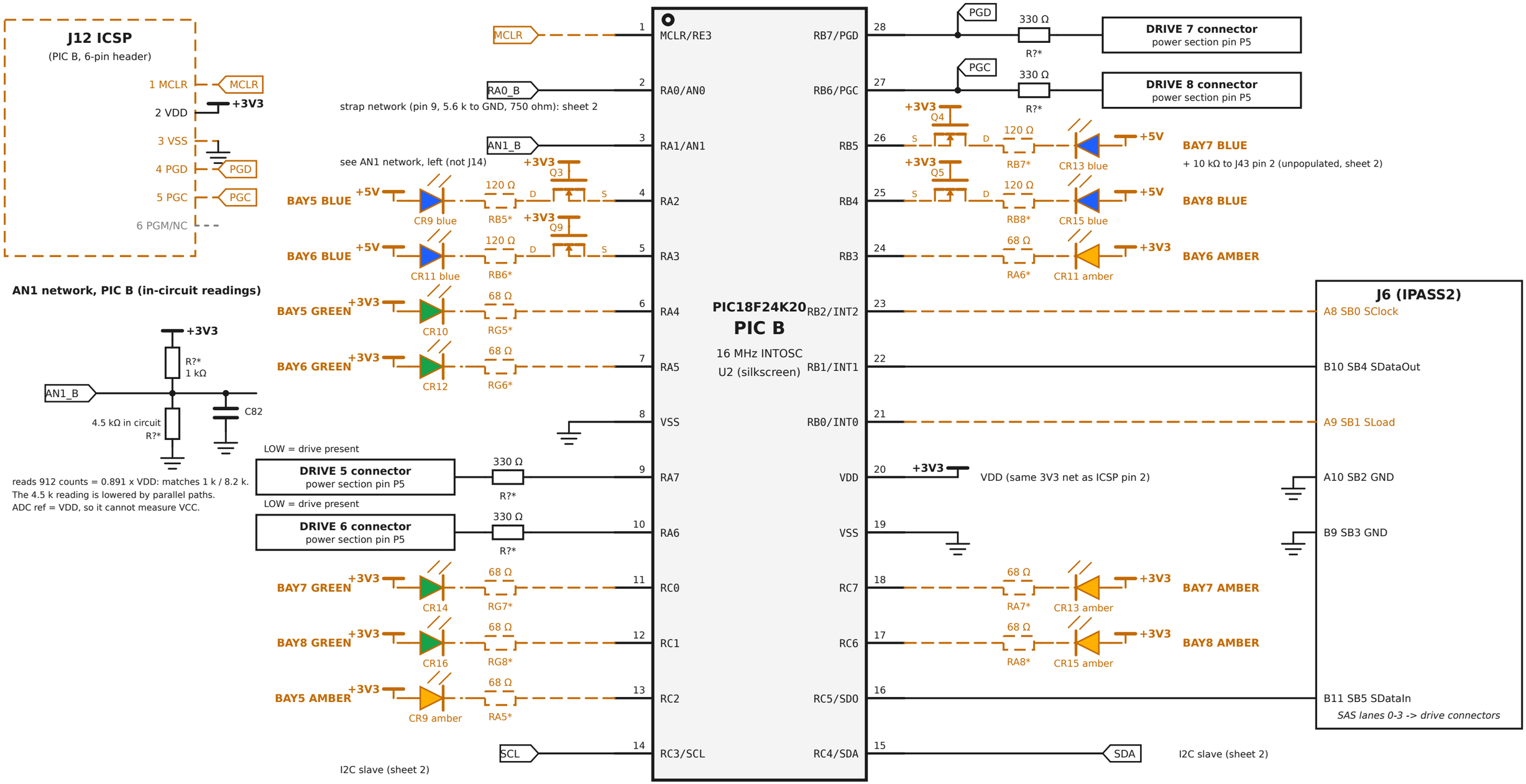
Reverse-engineered functional schematic - NOT the manufacturer's

Sheet 3/9: PIC A circuit (bays 1-4) - component level

Drawn 2026-11-05 from bench work 2026-11-04/05

PIC B circuit - PIC18F24K20, J6 (IPASS2) sideband, J12 ICSP, bays 5-8

Bays 5-8. Custom fw I2C 0x31 (backplane 1) / 0x33 (backplane 2). Stock fw 0x77 (strap network sets it).



BLUE: +5V -> LED -> 120 Ω -> FET drain. FET source = PIC pin, gate = +3V3 (fixed). GREEN / AMBER: +3V3 -> LED -> 68 Ω -> PIC pin. All LED pins are active low.
Solid = measured on bay 1 of PIC A only; every other bay is drawn dashed because its values are assumed identical. PGC/PGD share RB6/RB7 with drive-detect lines of bays 7 and 8.
CR1, CR3, CR5, CR7 / CR9, CR11, CR13, CR15 are the dual LEDs (blue and amber dies); CR2, CR4, CR6, CR8 / CR10, CR12, CR14, CR16 are the green LEDs.

WIRE / OUTLINE STYLE = HOW WELL IT IS KNOWN

- black solid: measured / verified on the real board
- amber dashed: inferred or assumed (e.g. copied from bay 1) - not measured
- grey dotted: not traced / unknown

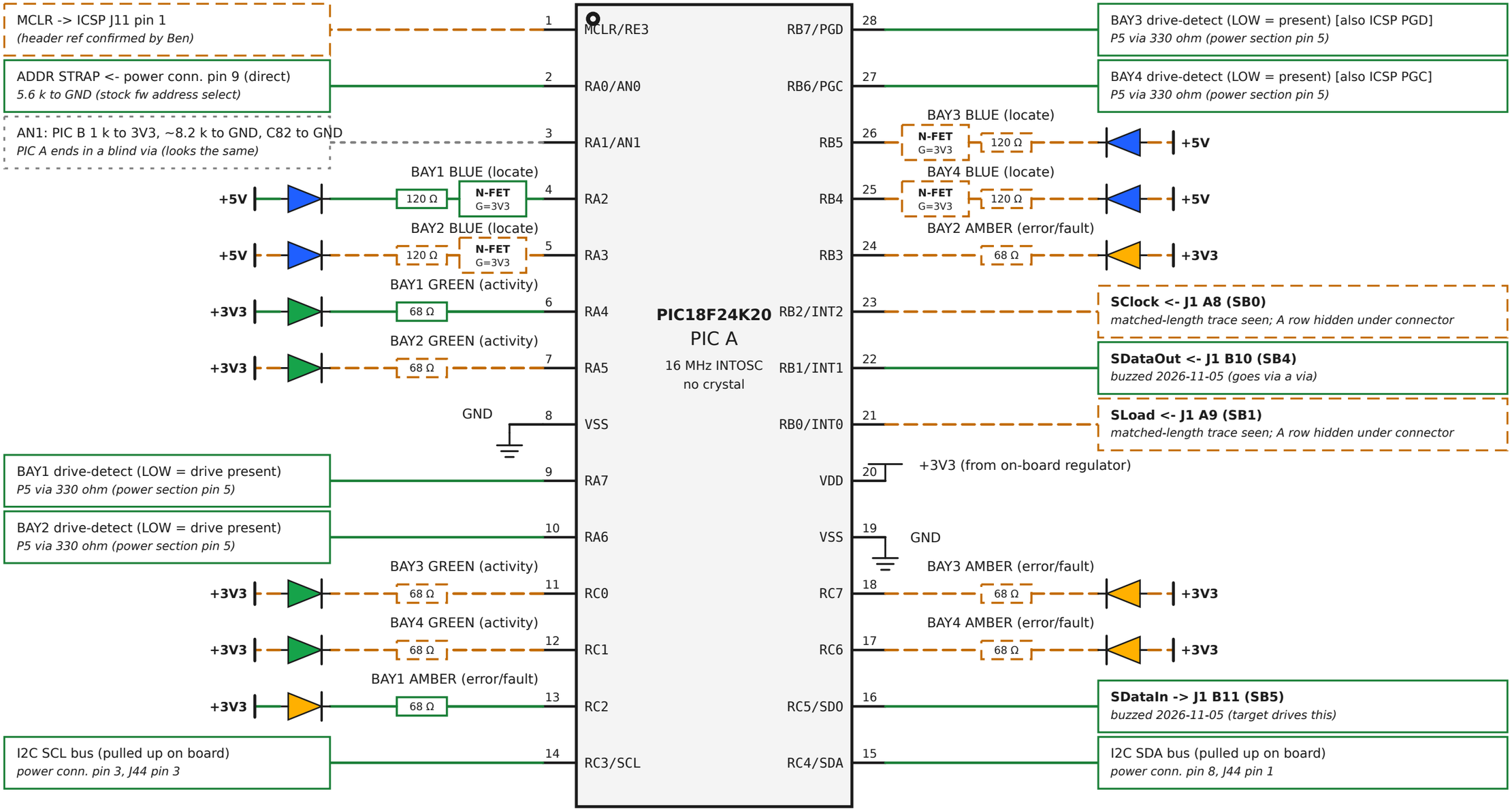
Designators J1, J6, J11, J12, J13, J14, J43, J44, U1, U2, Q and CR* are from the board (U1 = PIC A, U2 = PIC B).*
*Names ending in * (RB1*, RG2*, RA3* ...) are provisional labels given by this drawing.*

HP 8xSFF SAS backplane 496074-001 (DL380 G7)

Reverse-engineered functional schematic - NOT the manufacturer's
Sheet 4/9: PIC B circuit (bays 5-8) - component level
Drawn 2026-11-05 from bench work 2026-11-04/05

PIC A - PIC18F24K20 (28-pin SPDIP/SOIC numbering), bays 1-4

Bays 1-4. Custom fw I2C 0x30 (backplane 1) / 0x32 (backplane 2). Stock fw 0x76 with power-connector pin 9 grounded.



All LED pins are ACTIVE LOW (pin low = LED on). Solid = measured on bay 1 (PIC A); dashed = assumed identical for the other bays.

LINE STYLE = HOW WELL IT IS KNOWN

- verified on the real board (buzzed / hot-swapped / seen live)
- inferred (disassembly, standards, matched traces) - not tested
- not traced / unknown

SGPIO (pins 21/22/23/16): the stock firmware runs an INT2 (RB2) state machine = SFF-8485 target.
RB1 samples on SClock; per bay 3 bits in: Activity->GREEN, Locate->BLUE, Error->AMBER.
RC5 shifts out 3 bits per bay, the first being the drive-detect pin. The custom firmware does not use this link yet.
BLUE: +5V -> LED -> 120 ohm -> FET drain; FET source = PIC pin; gate = 3V3 (clamps the 5 V side away from the 3.3 V PIC pin).
GREEN, AMBER: +3V3 -> LED -> 68 ohm -> PIC pin directly (about 19 mA each). Pin 20 = same 3V3 net as ICSP pin 2.

HP 8xSFF SAS backplane 496074-001 (DL380 G7)

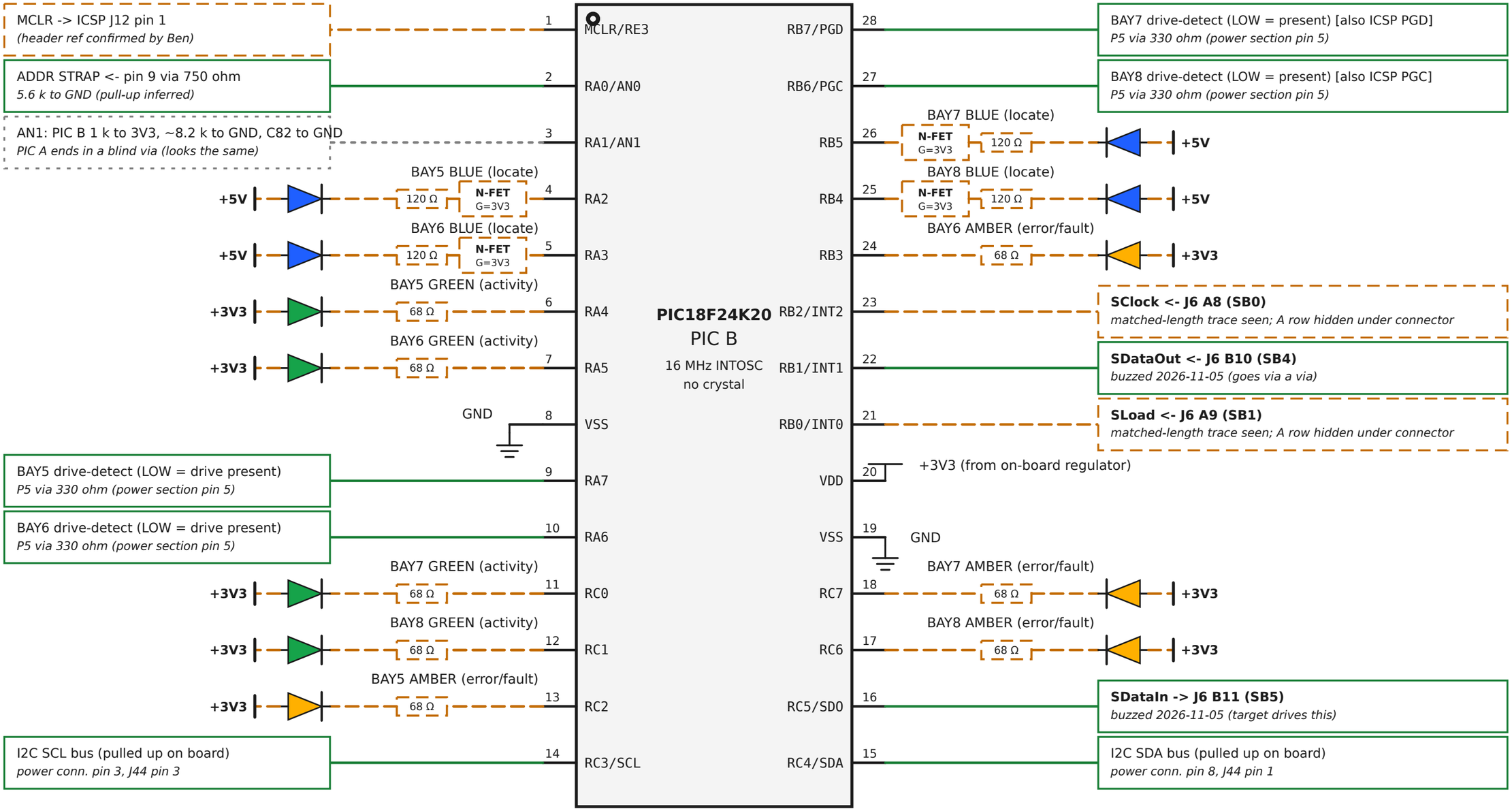
Reverse-engineered functional schematic - NOT the manufacturer's

Sheet 5/9: PIC A pin map (bays 1-4)

Drawn 2026-11-05 from bench work 2026-11-04/05

PIC B - PIC18F24K20 (28-pin SPDIP/SOIC numbering), bays 5-8

Bays 5-8. Custom fw I2C 0x31 (backplane 1) / 0x33 (backplane 2). Stock fw 0x77 (strap network sets it).



All LED pins are ACTIVE LOW (pin low = LED on). Solid = measured on bay 1 (PIC A); dashed = assumed identical for the other bays.

LINE STYLE = HOW WELL IT IS KNOWN

- verified on the real board (buzzed / hot-swapped / seen live)
- inferred (disassembly, standards, matched traces) - not tested
- not traced / unknown

SGPIO (pins 21/22/23/16): the stock firmware runs an INT2 (RB2) state machine = SFF-8485 target.
RB1 samples on SClock; per bay 3 bits in: Activity->GREEN, Locate->BLUE, Error->AMBER.
RC5 shifts out 3 bits per bay, the first being the drive-detect pin. The custom firmware does not use this link yet.
BLUE: +5V -> LED -> 120 ohm -> FET drain; FET source = PIC pin; gate = 3V3 (clamps the 5 V side away from the 3.3 V PIC pin).
GREEN, AMBER: +3V3 -> LED -> 68 ohm -> PIC pin directly (about 19 mA each). Pin 20 = same 3V3 net as ICSP pin 2.

HP 8xSFF SAS backplane 496074-001 (DL380 G7)

Reverse-engineered functional schematic - NOT the manufacturer's

Sheet 6/9: PIC B pin map (bays 5-8)

Drawn 2026-11-05 from bench work 2026-11-04/05

Connector pinouts (backplane end)

POWER / SIDEBAND CONNECTOR J13 (Mini-Fit Jr 10-pin)

1 +12 V	2 GND	3 I2C SCL	4 GND	5 +12 V
6 +5 V	7 GND	8 I2C SDA	9 STRAP (A, B 750 Ω)	10 +5 V

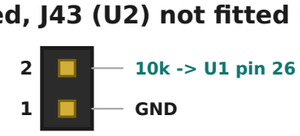
Verified: I2C on pins 3/8 (both PICs). Pin 9 goes straight to PIC A RA0 and through 750 Ω to PIC B RA0; each RA0 has 5.6 kΩ to GND.
+5 V -> TC1264-3.3 LDO (800 mA, SOT-223, marked 1264-33 / VDB1006) -> +3V3 for both PICs. +12 V feeds drive power.
The I2C bus hangs (SDA = SCL = 0) if 5 V is lost.

J44 I2C header

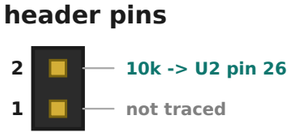
1	2	3
SDA	GND	SCL

Same bus as power-connector pins 3/8. ESP32: SDA=GPIO21, SCL=GPIO22, common GND.

J14 (U1) pins fitted, J43 (U2) not fitted (factory) - 0.1 inch header pins



J14 (U1)



J43 (U2, not fitted)

Pin 26 of each PIC is RB5 (also the blue LED FET of bay 3 / 7). No divider to ground.
Nothing plugs into either header in the server. Purpose unknown (see sheet 9).

ICSP headers J11 (PIC A) / J12 (PIC B) - standard 6-pin; header refs confirmed by Ben

1	2	3	4	5	6
MCLR	VDD	VSS	PGD	PGC	PGM/NC
PIC pin 1	PIC pin 20	PIC pin 8/19	RB7 pin 28	RB6 pin 27	

PGC/PGD share RB6/RB7 with the drive-detect pins of bays 3/4 (5-8): pull drives from those bays before programming.
The ICD4 holds the PIC in reset while attached and does NOT power the board.

LINE STYLE = HOW WELL IT IS KNOWN

- verified on the real board (buzzed / hot-swapped / seen live)
- inferred (disassembly, standards, matched traces) - not tested
- not traced / unknown

SFF-8087 (Mini SAS 4i) SIDEBAND - BACKPLANE END

Contacts 7..12 only; counted from the pin-1 end. Standard per T10 07-449r0 Table 35 (informative).

A row (hidden under the SMD body)

A7	A8	A9	A10	A11	A12
GND	SB0 SClock -> PIC 23 (RB2)	SB1 SLoad -> PIC 21 (RB0)	SB2 GND	SB6 reserved	GND

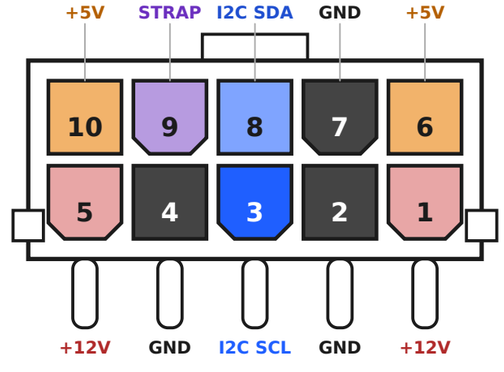
B row (exposed - buzzed)

B7	B8	B9	B10	B11	B12
GND	SB7 reserved	SB3 GND	SB4 SDataOut -> PIC 22 (RB1)	SB5 SDataIn -> PIC 16 (RC5)	GND

Verified 2026-11-05: B7, B9, B12 are ground; B10 goes to PIC pin 22; B11 goes to PIC pin 16.
A8/A9: a length-matched trace pair runs under the connector to PIC pins 23 and 21 - fits SClock/SLoad.

Other contacts (1-6, 13-18) are the 4 SAS lanes (Tx/Rx pairs + grounds), wired straight to the drive connectors.
J1 (IPASS1) feeds PIC A + bays 1-4; J6 (IPASS2) feeds PIC B + bays 5-8 (Ben, silkscreen).

POWER CONNECTOR J13 - Molex Mini-Fit Jr 2x5, mating-face view (Molex numbering)



Top row 10..6, bottom row 5..1 as in Molex's drawings (pin 6 above pin 1). Chamfered cavities: 9 confirmed, 4 and
Rotated 180 degrees this is the 'pin 1 above pin 6' view; check against the pin-1 mark on the board.

HP 8xSFF SAS backplane 496074-001 (DL380 G7)

Reverse-engineered functional schematic - NOT the manufacturer's
Sheet 7/9: Connectors and headers
Drawn 2026-11-05 from bench work 2026-11-04/05

Per-bay wiring and the SGPIO frame (same on every PIC)

PER-BAY PIN TABLE (verified by eye / hot-swap 2026-11-04; PIC pin numbers = 28-pin SPDIP/SOIC)

Bay (PIC A)	Bay (PIC B)	slot / mask bit	BLUE (locate)	GREEN (activity)	AMBER (error)	drive-detect (active low)
1	5	1 / bit0	RA2 pin 4	RA4 pin 6	RC2 pin 13	RA7 pin 9
2	6	2 / bit1	RA3 pin 5	RA5 pin 7	RB3 pin 24	RA6 pin 10
3	7	3 / bit2	RB5 pin 26	RC0 pin 11	RC7 pin 18	RB7 pin 28
4	8	4 / bit3	RB4 pin 25	RC1 pin 12	RC6 pin 17	RB6 pin 27

Green + amber share one 4-pin LED element per bay; blue is a separate LED. Green+amber together look green/purple. Pins are ACTIVE LOW.

SGPIO FRAME AS SEEN BY THE STOCK FIRMWARE (inferred from the INT2 state machine at 0x1B92-0x1E5E; not captured live)

RB2 (SClock) interrupts on both edges; states alternate: [sample RB1 -> drive an LED pin] on one edge, [drive RC5] on the other. RB0 (SLoad) high mid-frame forces a resync.

order	bay	SDataIn out (RC5) backplane -> HBA	SDataOut in (RB1) HBA -> backplane	LED pin driven
1	bay 1 / 5	bit A: drive-detect pin RA7 (RAM copy)	bit 0 -> GREEN activity	RA4
2	bay 1 / 5	bit B: RAM flag	bit 1 -> BLUE locate (OR I2C locate mask)	RA2
3	bay 1 / 5	bit C: RAM flag	bit 2 -> AMBER error	RC2
4	bay 2 / 6	bit A: drive-detect pin RA6	bit 0 -> GREEN	RA5
5	bay 2 / 6	bit B: RAM flag	bit 1 -> BLUE (OR I2C locate mask)	RA3
6	bay 2 / 6	bit C: RAM flag	bit 2 -> AMBER	RB3
7	bay 3 / 7	bit A: drive-detect pin RB7	bit 0 -> GREEN	RC0
8	bay 3 / 7	bit B: RAM flag	bit 1 -> BLUE (OR I2C locate mask)	RB5
9	bay 3 / 7	bit C: RAM flag	bit 2 -> AMBER	RC7
10	bay 4 / 8	bit A: drive-detect pin RB6	bit 0 -> GREEN	RC1
11	bay 4 / 8	bit B: RAM flag	bit 1 -> BLUE (OR I2C locate mask)	RB4
12	bay 4 / 8	bit C: RAM flag	bit 2 -> AMBER	RC6

Matches SFF-8485 (per drive: Activity, Locate, Error). Direction: SClock/SLoad/SDataOut are driven by the HBA (initiator); SDataIn is driven by the backplane (target).
Open: bit polarity, which RAM flags feed the 'B'/'C' outgoing bits, clock rate of the real HBA (a 9211-8i in IT mode may not drive the link at all).
Custom firmware v2 (built, not yet flashed) has a passive capture mode to settle this (sheet 9).

LINE STYLE = HOW WELL IT IS KNOWN

- verified on the real board (buzzed / hot-swapped / seen live)
- inferred (disassembly, standards, matched traces) - not tested
- not traced / unknown

HP 8xSFF SAS backplane 496074-001 (DL380 G7)

Reverse-engineered functional schematic - NOT the manufacturer's
Sheet 8/9: Per-bay pin table and SGPIO frame
Drawn 2026-11-05 from bench work 2026-11-04/05

Firmware interfaces and open items

CUSTOM FIRMWARE I2C REGISTER MAP (100 kHz, pointer + auto-increment, clock stretching)

reg	meaning
0x00 / 01 / 02	ID 0xB0 / firmware version (2) / chip index (0 = bays 1-4, 1 = bays 5-8)
0x10 / 11 / 12	BLUE / GREEN / AMBER LED mask, bit0 = first bay of the PIC, 1 = on (RW)
0x20 / 21 / 22	PORTA / PORTB / PORTC pin levels. Drive present = bit CLEAR
0x30-0x33	AN0 lo,hi / AN1 lo,hi (10-bit, 3.3 V ref); AN1 ~911 counts (source not found)
0x40-0x44	TRISA/B/C, WPUB, RBPU (RC3/RC4/RB6/RB7 forced input)
0x4F, 0x50-0x52	raw mode; direct LATA/B/C writes
0x60-0x63, 0x65, 0x66	NEW (v2, unflashed): SClock edge count, SLoad count, capture state, enable/arm, clear
0x70-0x8F	NEW: 32 raw PORTB samples, one per SClock rising edge (bit0 SLoad, bit1 SDataOut)

Addresses: backplane 1 (right cage B) PIC A 0x30, PIC B 0x31; backplane 2 (left cage A) PIC A 0x32, PIC B 0x33.
Stock firmware: address from AN0 voltage (pin 9 grounded -> 0x76 / 0x77); never send D8/0A (EEPROM write) or type 0xFF (bootloader key).
Restore a stock image: ipecmd.sh -TPICD4 -P18F24K20 -F<original>.hex -M (NEVER -ME). Originals: dumps/pic?_original_2026-11-04.hex

OPEN ITEMS / NOT YET KNOWN

* A8 / A9 pad-level confirmation (A row hidden); signals inferred from the matched-trace pair and the standard.
* SGPIO polarity and the meaning of the two 'RAM flag' outgoing bits; live capture needed (HBA or ESP32 as initiator).
* Purpose of J14 / J43 (10 k from pin 2 to RB5 of each PIC).
* AN1 (RA1): PIC B = 1 k / ~8.2 k divider + C82 to GND; PIC A ends in a blind via but looks the same. Temperature test pending once the cages are installed (ID strap vs sensor).
* PIC B RA0 pull-up (~680 ohm?) is inferred only.
* LED network measured on bay 1 only (68 / 120 ohm, blue on 5 V + FET, green/amber on 3V3); others assumed.
* FET part: marked 701 (datasheet 2N7002L = 702).
* Whether a 9211-8i (IT) drives the sideband at all.
* Regulator = TC1264-3.3 (800 mA, SOT-223); PIC decoupling not read.
* Fans, 1-Wire sensors, remote-power parts: see the separate ESP32 bay-controller schematic (not this board).

HOW THIS DRAWING WAS BUILT

Pin functions come from the stock-firmware disassembly (tools/pic18dis.py) and were then checked on the board:
LEDs by eye, drive-detect by hot-swapping drives, I2C by live scanning, the SFF-8087 B row by buzzing out.
No full netlist of the board exists: passives, the regulator and the SAS lane routing were not traced.
Source files: docs/BACKPLANE_REFERENCE.md, custom_fw/main.c, dumps/*.hex. Regenerate this PDF with hardware/backplane_schematic/gen_backplane_schematic.py.

LINE STYLE = HOW WELL IT IS KNOWN

- verified on the real board (buzzed / hot-swapped / seen live)
- inferred (disassembly, standards, matched traces) - not tested
- not traced / unknown

HP 8xSFF SAS backplane 496074-001 (DL380 G7)

Reverse-engineered functional schematic - NOT the manufacturer's
Sheet 9/9: Firmware interfaces and open items
Drawn 2026-11-05 from bench work 2026-11-04/05